

Fig. 3

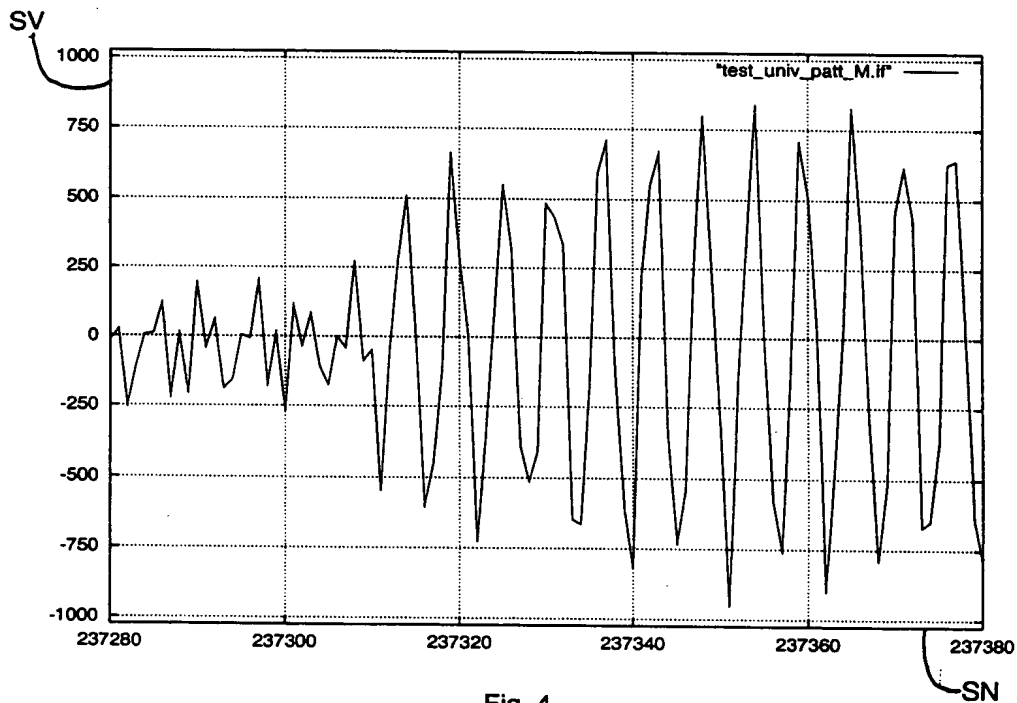


Fig. 4

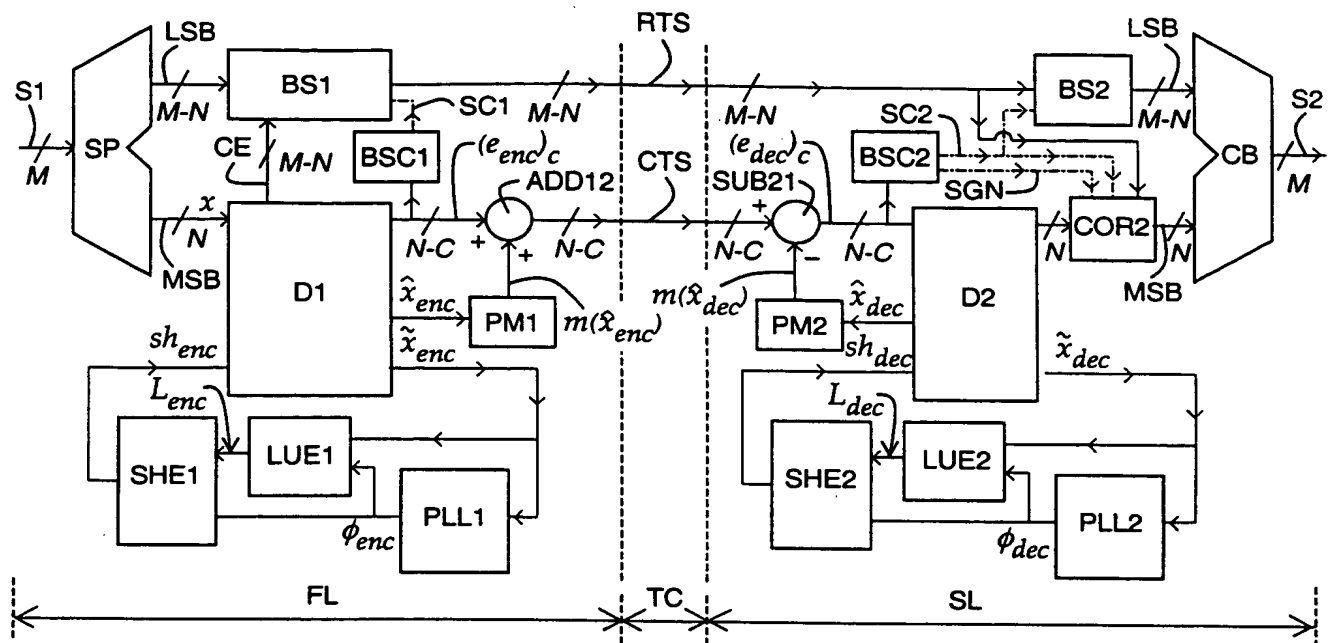


Fig. 5

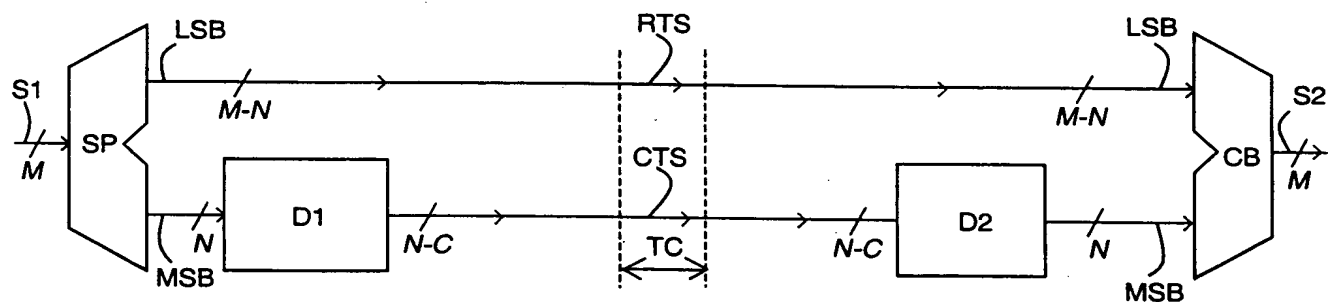
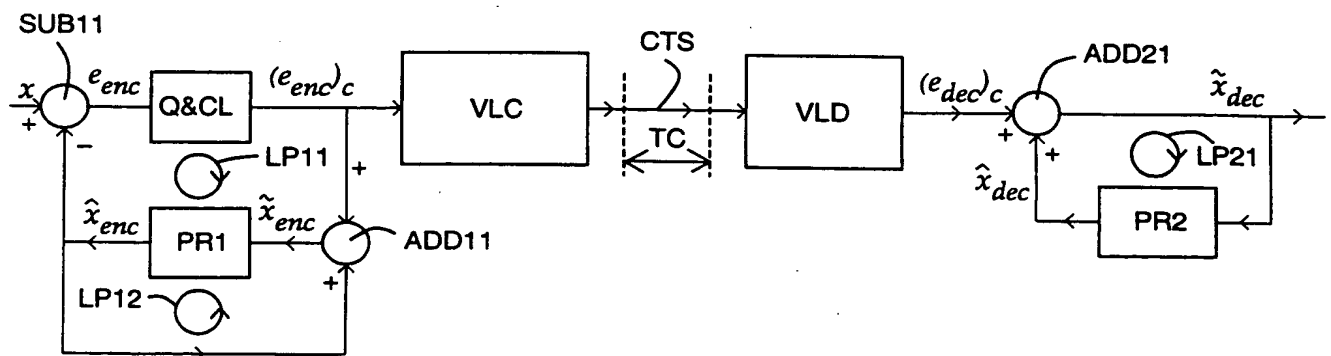


Fig. 6



PRIOR ART
 Fig. 7

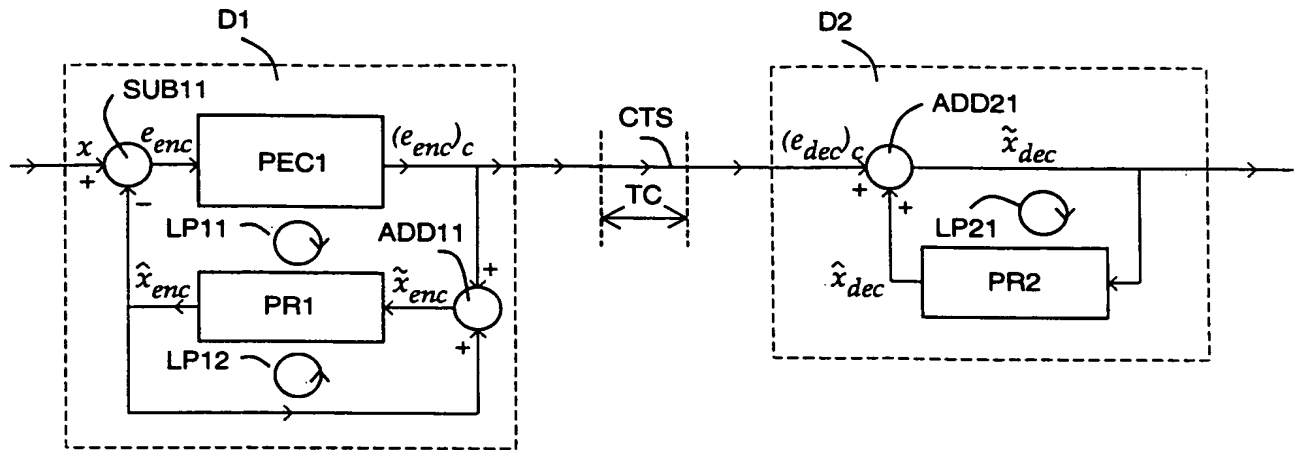


Fig. 8

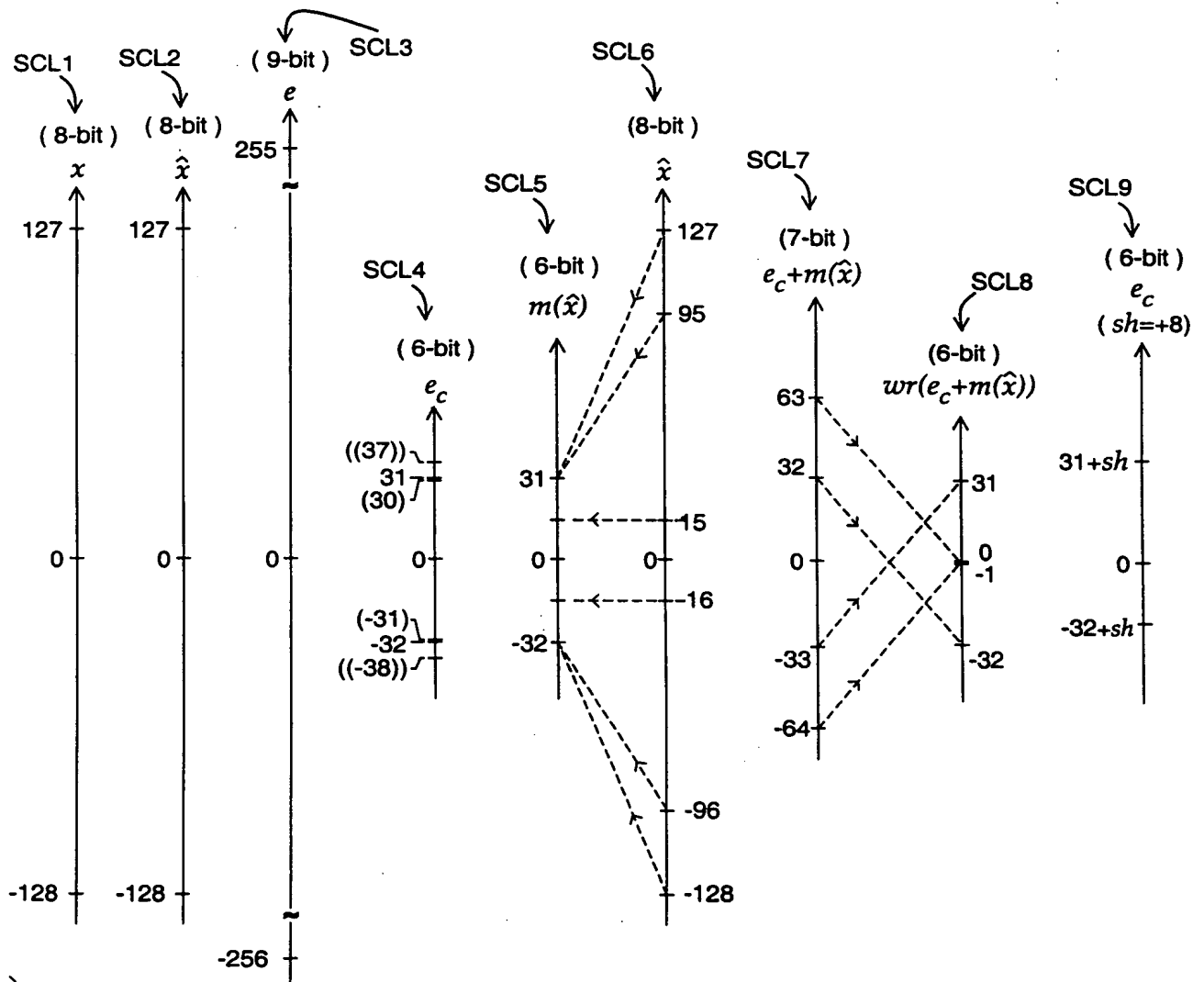


Fig. 9

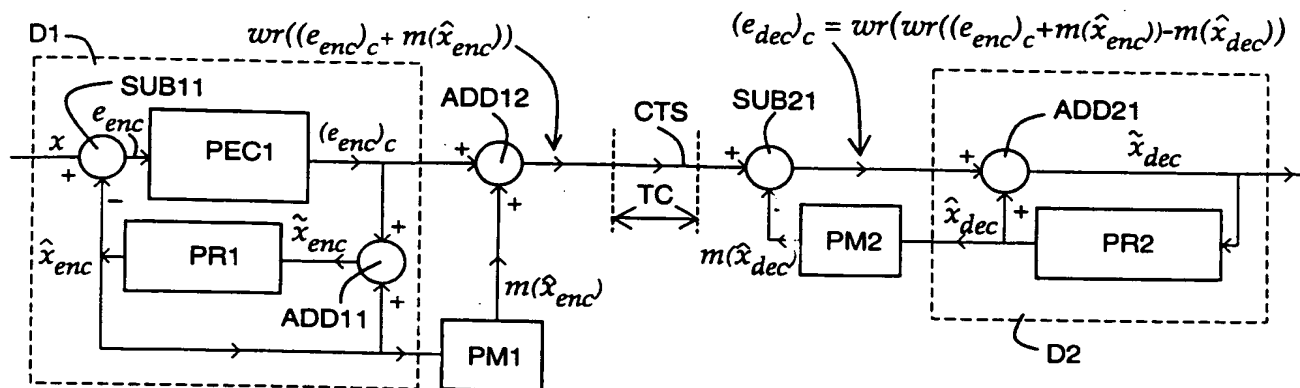


Fig. 10

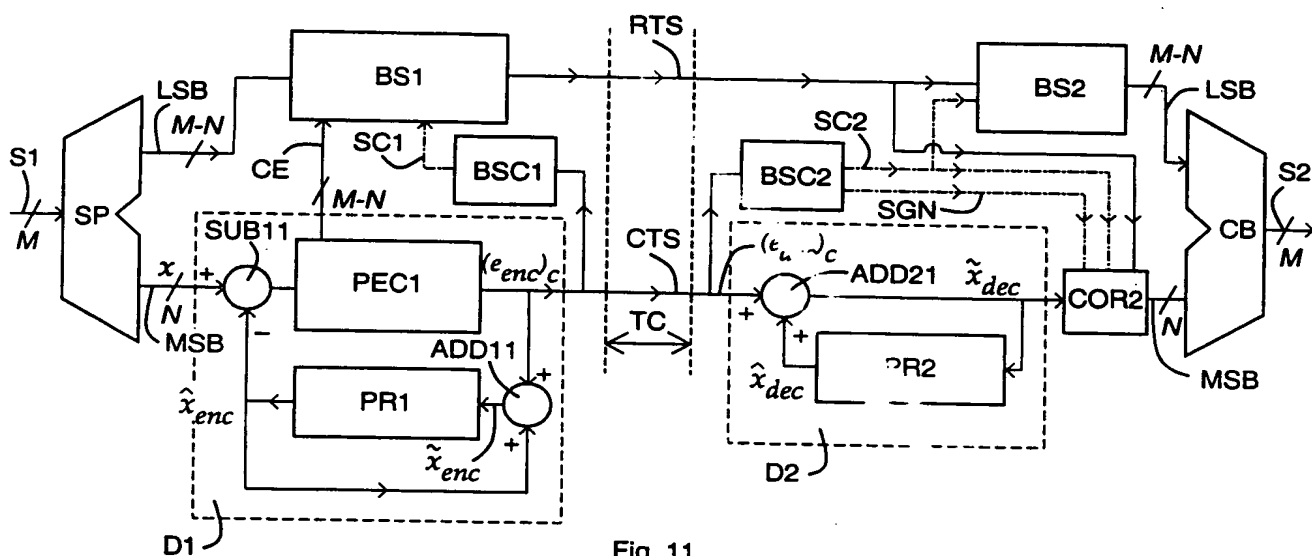


Fig. 11

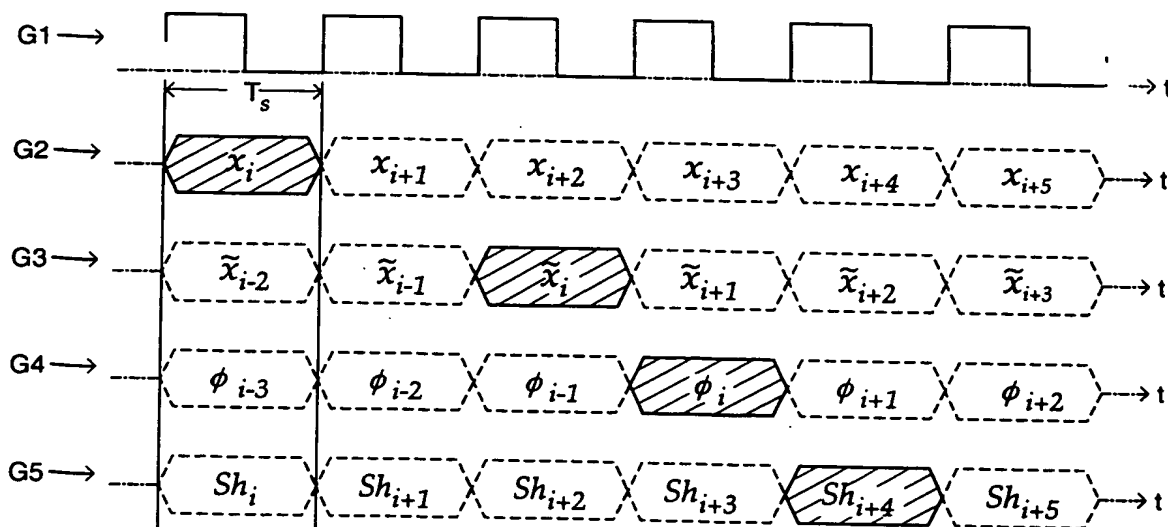


Fig. 20

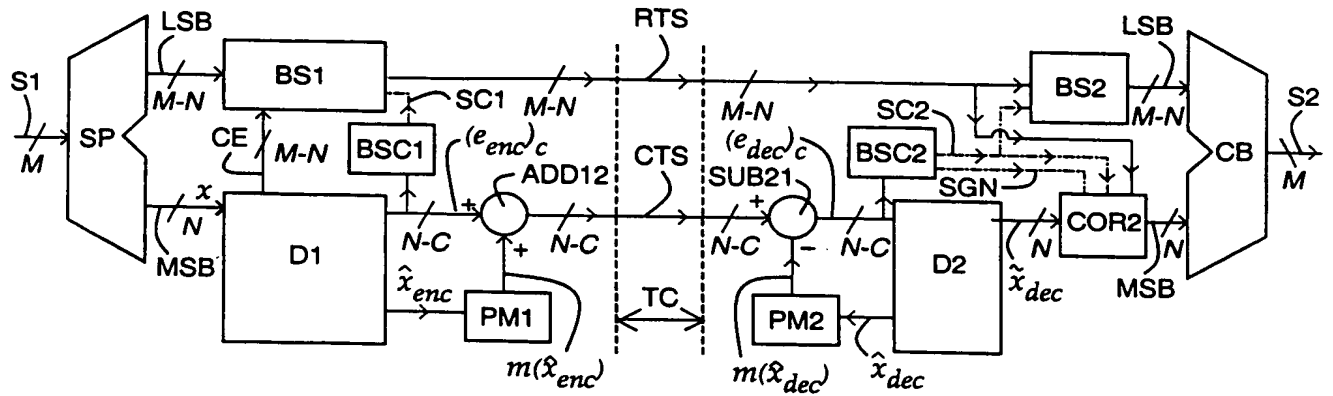


Fig. 12

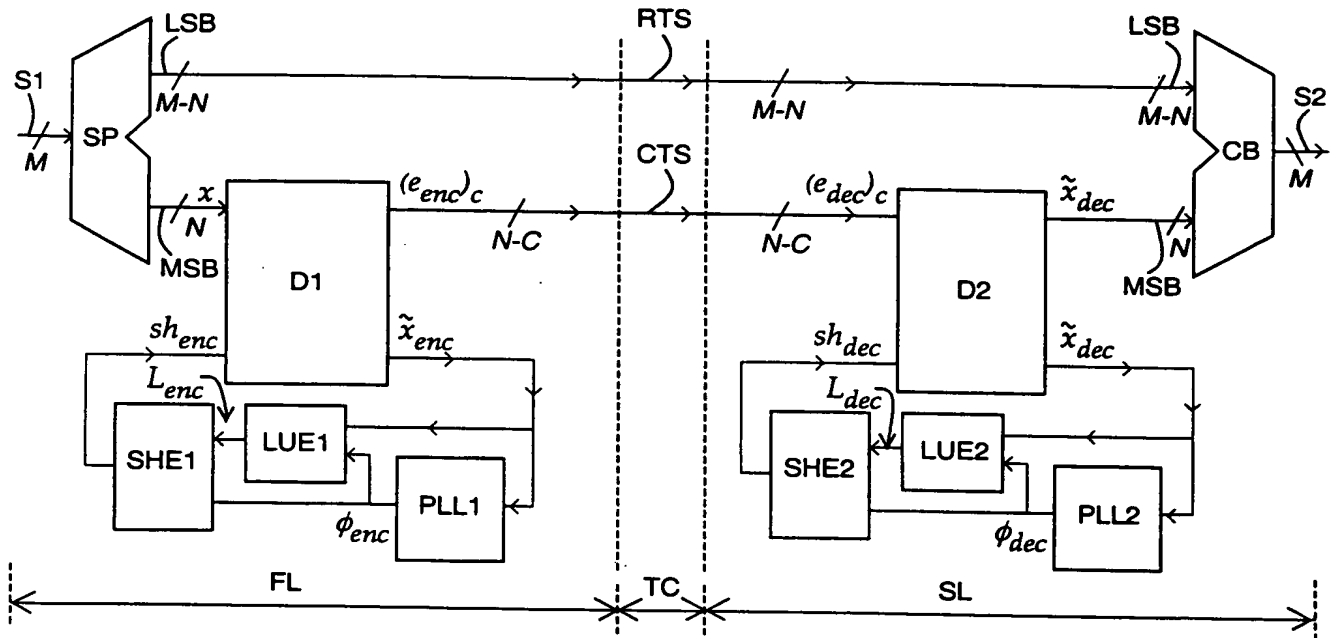


Fig. 15

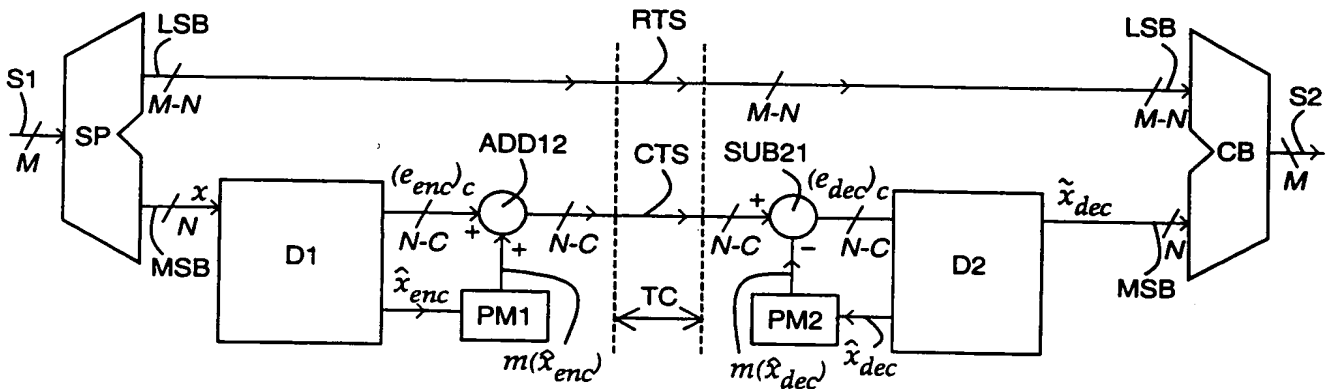
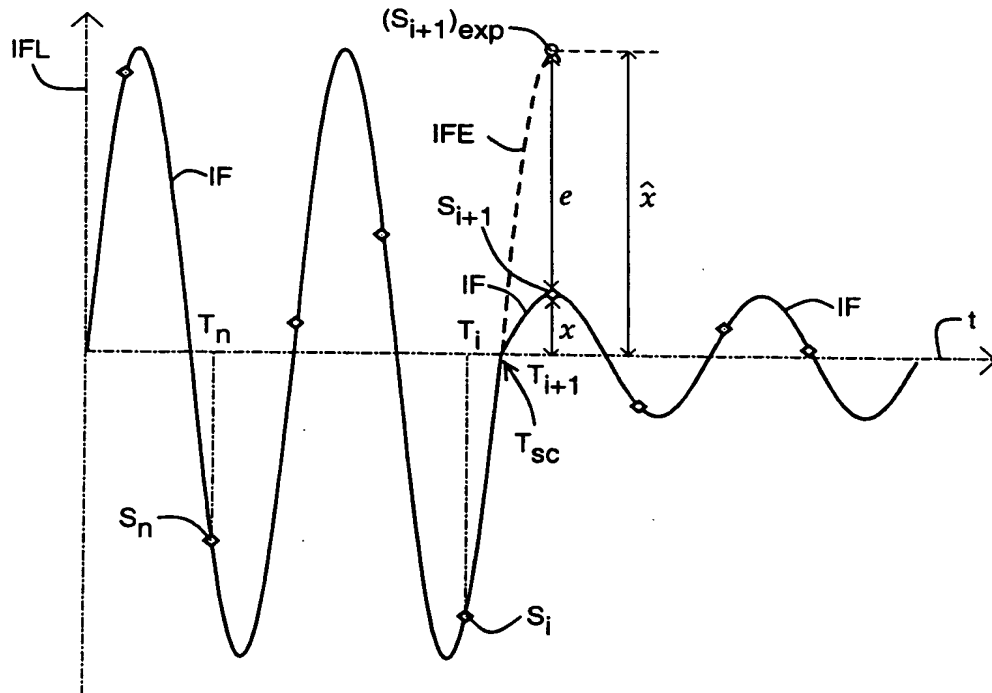


Fig. 21



The diagram shows the internal structure of the SHE, enclosed in a dashed box. It includes the following components and connections:

- Inputs:**
 - L : A signal input that branches to the left input of **REG2** and the top input of **SHC**.
 - ϕ : A signal input that enters a block labeled $\sin(\phi + 4\Delta\phi)$.
- Internal Blocks:**
 - REG2**: A register that receives L and outputs to the top input of **SHC**.
 - Q**: A block that receives the output of the $\sin(\phi + 4\Delta\phi)$ block and outputs to the bottom input of **SHC**.
 - SHC**: A central processing block that receives inputs from **REG2** and **Q**, and produces the output sh .
- Output:**
 - sh : The final output signal from the **SHC** block.

The diagram illustrates the architecture of the proposed PLL-based digital PLL (DPLL) for both encoder and decoder paths. The encoder path (D1) and decoder path (D2) are shown side-by-side.

Encoder Path (D1):

- The input signal x is processed by a series of subtractors (SUB11, SUB12) and an adder (ADD13) to produce the error signal e_{enc} .
- The error signal e_{enc} is then processed by a phase accumulator (LUE1) to produce the phase ϕ_{enc} .
- The phase ϕ_{enc} is fed into a phase-locked loop (PLL1) and a phase accumulator (LUE1) to produce the phase ϕ_{enc} .
- The phase ϕ_{enc} is then used to generate the error signal e_{enc} via a phase accumulator (LUE1) and a phase-locked loop (PLL1).
- The error signal e_{enc} is then processed by a phase accumulator (LUE1) to produce the phase ϕ_{enc} .
- The phase ϕ_{enc} is then used to generate the error signal e_{enc} via a phase accumulator (LUE1) and a phase-locked loop (PLL1).

Decoder Path (D2):

- The input signal $(e_{dec} - sh_{dec})c$ is processed by a series of subtractors (SUB21, SUB22) and an adder (ADD23) to produce the error signal e_{dec} .
- The error signal e_{dec} is then processed by a phase accumulator (LUE2) to produce the phase ϕ_{dec} .
- The phase ϕ_{dec} is fed into a phase-locked loop (PLL2) and a phase accumulator (LUE2) to produce the phase ϕ_{dec} .
- The phase ϕ_{dec} is then used to generate the error signal e_{dec} via a phase accumulator (LUE2) and a phase-locked loop (PLL2).
- The error signal e_{dec} is then processed by a phase accumulator (LUE2) to produce the phase ϕ_{dec} .
- The phase ϕ_{dec} is then used to generate the error signal e_{dec} via a phase accumulator (LUE2) and a phase-locked loop (PLL2).

Fig. 19

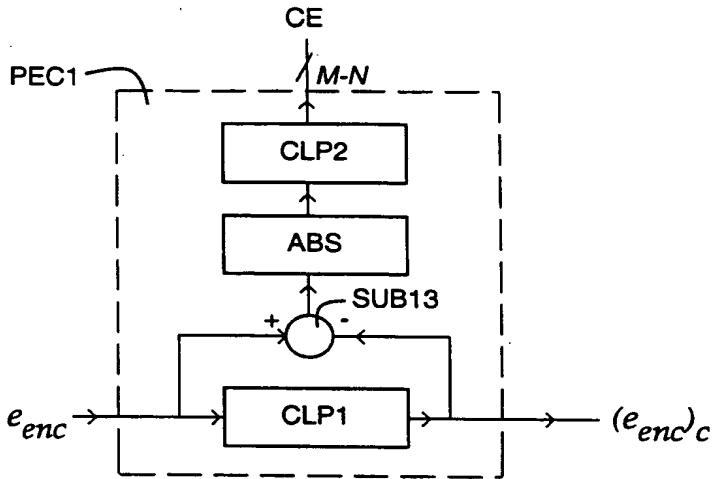


Fig. 22

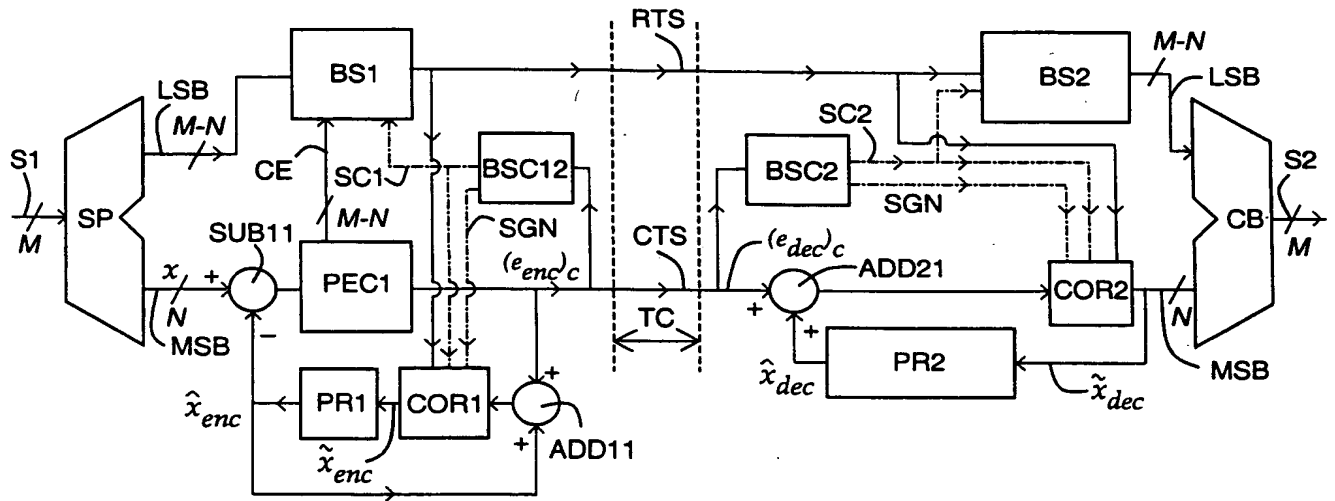


Fig. 23